SMALL-SIGNAL RF YIELD ANALYSIS OF MMIC CIRCUITS BASED ON PHYSICAL DEVICE PARAMETERS

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ABSTRACT

This paper describes a technique for computing small-signal RF yield of monolithic microwave integrated (MMIC) circuits based on the sensitivity of electrical model parameters to physical device parameters. Because GaAs MMICs are increasingly being used in large scale production programs, the producibility of a given design must be considered at the beginning of the design process. The RF yield analysis approach to be described uses key MMIC device physical variables and computed sensitivities of electrical model parameters to those variables.

INTRODUCTION

In previous work, the statistical design of microwave circuits has focused on the determination of parametric variation of the GaAs FET devices only. FET equivalent circuit model parameter statistics were studied by Purviance et. al. [1]. This work demonstrated that data on the statistics of FET parameters is not sufficient to characterize the statistics on S-parameters. Instead Purviance et.al. proposed the use of the "Truth Model" which is based on performing a statistical analysis using the original FET database. Campbell [5] improved the "Truth Model" by interpolating between data points in the FET database. These methods are accurate but have the disadvantage of requiring a large database for each separate FET.

In this paper, we use a statistical model for GaAs MMICs which is based on the sensitivity of electrical model parameters to physical device parameters involved in the processing of MMIC circuits. This method is flexible and is easily applied to FETs and other MMIC circuit elements.

There are several advantages to this approach that include (1) using a statistically independent variable set, (2) RF yield is easily estimated for different device profiles, (3) passive and active MMIC circuit parameters are included in the analysis, (4) circuit variability can be traced to process control points, (5) the approach makes use of a large database of device physical measurements which are made on every wafer, and (6) the approach can be implemented using almost any nominal FET model.

APPROACH

A block diagram of the yield estimation process is shown in Figure 1. The approach consists of combining the statistical variation of physical device parameters and sensitivity equations for each microstrip or FET device electrical model parameter with a linear circuit file describing a given MMIC device. The sensitivity equations relate the key electrical parameters of the MMIC circuit to the physical process

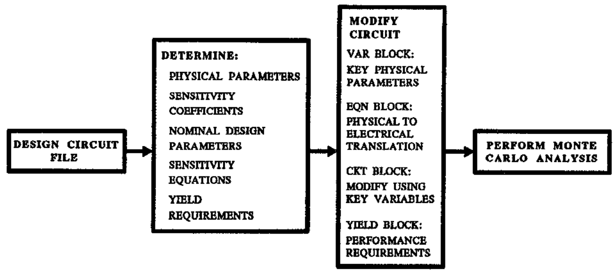

Figure 1. RF Yield Prediction Process

variables. In this work, the physical device and microstrip parameters as shown in Table 1 are included in the VAR block of a Touchstone/Libra circuit file while the device and microstrip sensitivity equations are described in the EQN block. The data for the parameters included in these blocks consists of the parameter mean value and standard deviations which are routinely derived from GaAs foundry data on each wafer. Additionally, a yield specification for the MMIC circuit is specified in the YIELD block. Once the VAR, EQN, and YIELD blocks are defined, the Monte Carlo analysis features of Touchstone/Libra are used to compute the MMIC device yield. Variations of the Monte Carlo analysis that can be done include either computing performance yield versus a specification or computing a histogram of performance to determine a performance mean and standard deviation.

SENSITIVITY EQUATIONS AND COEFFICIENTS

In the analysis, the relationship of device electrical model parameters to the physical parameters is described by a set of sensitivity equations which are first order Taylor series approximations. As an example, the sensitivity equation for Cgs is shown below.

TABLE 1. PHYSICAL MMIC DEVICE VARIABLES

	Parameter	Symbol	Std. Dev.
Linewidth	Isolation	DLWI	0.100 µm
Parameters	Ohmic	DLWOH	0.005 µm
	TaN	DLWTAN	0.030 µm
	TaN Contact	DLWTAN	0.030 µm
	TF Resistor	DLWTF	0.070 µm
	First Metal	DLWFM	0.030 µm
	Cap Top Plate	DLWTP	0.030 µm
	Plated Metal	DLWPM	0.700 µm
GaAs Resistors	Activation	DA	0.100
	Surface Potential	DPHIS	0.110
	Contact Resistance	DRC	0.059
MIM Capacitors	Cap Top Plate	DLWTP	0.030 µm
	Capacitance/Area	CMIM	7pF/mm^2
FETs	Gate Length	DLG	0.0395
	Narrow Recess	DLNR	0.052
	Narrow Recess	DISAT	0.030
	Wide Recess	DLWR	0.096
	Wide Recess	DISATW	0.020
	Source-Drain	DLSD	0.047
	Gate-Drain	DLGS	0.081
	Isolation	DLWI	0.100
	Activation	DA	0.100
	Surface Potential	DPHIS	0.110
	Contact Resistance	DRC	0.059

$$Cgs = Cgs_o*\left[1 + S_{WI}^{Cgs}*\left(\frac{DLWI}{WGF}\right) + S_{LG}^{Cgs}*DLG + S_{A}^{Cgs}*DA + S_{ISAT}^{Cgs}*DISAT\right]$$

In this equation, Cgs_o is the nominal or design value. The other terms consist of sensitivity coefficients (i.e. S_{Lg}^{Cgs}) and physical parameter percent standard deviations. Standard deviations for the physical variables considered are shown in Table 1. During yield analysis, the parameter Cgs will vary randomly as a function of the physical variables shown. MMIC circuits with different device profiles can easily be analyzed by changing the appropriate sensitivity coefficients. Other intrinsic FET parameters are described in a similar manner using the equations in Table 2.

The variation in MMIC performance due to other circuit elements such as MIM capacitors and GaAs resistors can also be computed. The sensitivity equations for these two circuit elements are given below.

$$C = Cmim*(W0+DLWTP)*(L0+DLWTP)$$

where Cmim = capacitance/unit area

$$R = Rs_o*\left(1+S_{A}^{Rs}*DA+S_{PHIS}^{Rs}*DPHIS\right)\frac{(L0-DLWOH)}{(W0+DLWOH)} + \frac{2*Rc(1+DRC)}{(W0+DLWISO)}$$

where Rs_o = GaAs sheet resistance
Rc = contact resistance

TABLE 2. FET SENSITIVITY EQUATIONS

$$Cgs = Cgs_o*\left[1 + S_{WI}^{Cgs}*\left(\frac{DLWI}{WGF}\right) + S_{LG}^{Cgs}*DLG + S_{LSD}^{Cgs}*DLSD\right] + Cgs_o*\left(S_{A}^{Cgs}*DA + S_{ISAT}^{Cgs}*DISAT + S_{PHIS}^{Cgs}*DPHIS\right)$$

$$Rg = Rg_o*\left(1 + S_{LG}^{Rg}*DLG\right)$$

$$Cgd = Cgd_o*\left[1 + S_{WI}^{Cgd}*\left(\frac{DLWI}{WGF}\right) + S_{LG}^{Cgd}*DLG + S_{LSD}^{Cgd}*DLSD + S_{LGS}^{Cgd}*DLGS\right]$$

$$gm = gm_o*\left[1 + S_{WI}^{gm}*\left(\frac{DLWI}{WGF}\right) + S_{A}^{gm}*DA + S_{ISAT}^{gm}*DISAT + S_{PHIS}^{gm}*DPHIS\right]$$

$$T = T_o*\left(1 + S_{LG}^{T}*DLG\right)$$

$$Rs = Rs_o*\left[1+S_{WI}^{Rs}*\left(\frac{DLWI}{WGF}\right)+S_{LG}^{Rs}*DLG+S_{LNR}^{Rs}*DLNR+S_{LWR}^{Rs}*DLWR+S_{LSD}^{Rs}*DLSD\right] +Rs_o*\left(S_{A}^{Rs}*DA+S_{ISAT}^{Rs}*DISAT+S_{ISATW}^{Rs}*DISATW+S_{PHIS}^{Rs}*DPHIS+S_{RC}^{Rs}*DRC+S_{LGS}^{Rs}*DLGS\right)$$

$$Cds = Cds_o*\left[1 + S_{WI}^{Cds}*\left(\frac{DLWI}{WGF}\right) + S_{LSD}^{Cds}*DLSD\right]$$

$$Rds = Rds_o*\left[1 + S_{WI}^{Rds}*\left(\frac{DLWI}{WGF}\right)\right]$$

$$Rd = Rd_o*\left[1+S_{WI}^{Rd}*\left(\frac{DLWI}{WGF}\right)+S_{LG}^{Rd}*DLG+S_{LNR}^{Rd}*DLNR+S_{LWR}^{Rd}*DLWR+S_{LSD}^{Rd}*DLSD\right] +Rd_o*\left(S_{A}^{Rd}*DA+S_{ISAT}^{Rd}*DISAT+S_{ISATW}^{Rd}*DISATW+S_{PHIS}^{Rd}*DPHIS+S_{RC}^{Rd}*DRC + S_{LGS}^{Rd}*DLGS\right)$$

where

$$S_{\alpha}^{\beta} = \frac{\alpha_o}{\beta_o}\frac{\partial\beta}{\partial\alpha}$$

β = electrical parameter
α = physical parameter

A variety of microstrip circuit elements can be described by similar sensitivity equations and are limited only by the availability of a suitable model and the total number of variables and equations needed to describe a MMIC circuit. Circuit elements included in the RF yield model to date have included FETs, Metal-Insulator-Metal (MIM) capacitors, thin film resistors, critical transmission lines, open circuit stubs, and substrate parameters.

To perform a yield analysis the sensitivity of electrical model parameters (i.e. the sensitivity coefficients) as a function of physical process parameters is needed. The sensitivity coefficients for the intrinsic FET parameters Cgs, Cgd, Cds, gm, and sheet resistance were computed using a device physics based program developed at Texas Instruments called FETMOD. For the model parameters Rds, Rd, Rs, and Rg, the sensitivity coefficients were computed manually using data derived from the GaAs foundry database. An example of the sensitivity coefficients for a low-noise high current FET profile is shown in Table 3.

NUMERICAL EXAMPLE

To demonstrate the accuracy of the proposed approach, the following example RF yield analysis of a broadband low-noise MMIC distributed amplifier is described and compared to measured data. The low-noise amplifier shown in Figure 2 has a total gate periphery of 756 µm and is

TABLE 3. LOW-NOISE HIGH CURRENT PROFILE SENSITIVITY COEFFICIENTS

	DLWI	DLG	DLNR	DLWR	DLSD	DA	DISAT	DISATW	DPHIS	DPHIS	DLGS
Rg	0.0	-1.18	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Cgs	1.0	0.81	0.0	0.0	-0.02	0.24	-0.54	0.0	-0.25	0.0	0.0
Ri	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Cgd	1.0	0.28	0.0	0.0	-0.25	0.0	0.0	0.0	0.0	0.0	0.24
Ci	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
gm	1.0	0.0	0.0	0.0	0.0	0.30	-0.68	0.0	-0.32	0.0	0.0
T	0.0	1.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Rs	-1.0	-0.08	0.09	0.12	0.58	-0.19	-0.03	-0.20	0.07	0.12	0.54
Cds	1.0	0.0	0.0	0.0	-0.22	0.0	0.0	0.0	0.0	0.0	0.0
Rds	-1.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Rd	-1.0	-0.07	0.09	0.11	0.54	-0.18	-0.03	-0.18	0.06	0.11	-0.50

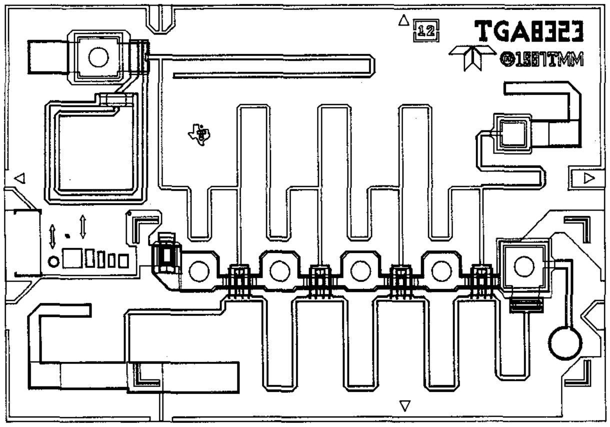

Figure 2. Broadband Low-Noise Distributed Amplifier

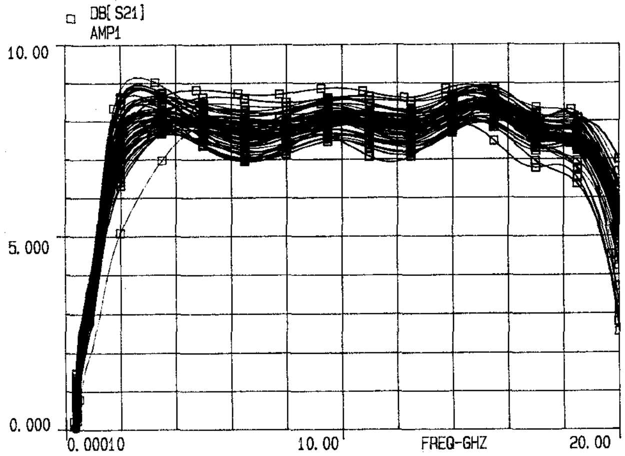

Figure 3. Predicited Small-Signal Gain Variation

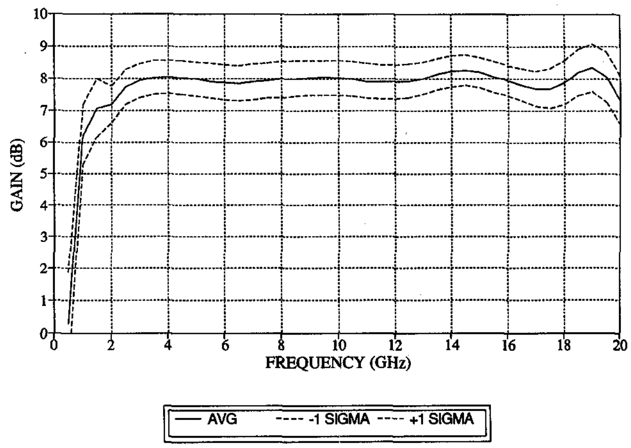

Figure 4. Measured Small-Signal Gain Variation

comprised of four single-gate FETs with gate widths of 189 µm each. This MMIC amplifier was fabricated using TI standard (low-noise high current) ion-implant material (peak doping approximately 1.0 X 10^{18} cm^{-3}). The physical parameter standard deviations and sensitivity coefficients for this material type are given in Tables 1 and 2. The RF yield model for this MMIC amplifier includes models of the FETs, critical transmission lines, MIM capacitors, GaAs resistors, and inductive bond wires.

After modifying the design circuit file and adding the physical variable standard deviations, sensitivity equations, and yield requirements, a Monte Carlo analysis was performed on the low-noise amplifier. The predicted versus measured statistical variations in small-signal gain are shown in Figures 3 and 4. For the computed performance, 50 trial sweeps were used while the measured data was derived from approximately 200 devices. To compute an accurate mean and standard deviation, a performance histogram of gain (Figure 5) using 5000 trials was computed at 10 GHz. In summary the predicted mean and standard deviation in gain at 10 GHz is 8.11 dB $\pm$0.32 dB and the measured mean and standard deviation was 8.01 dB $\pm$0.54 dB. The predicted standard

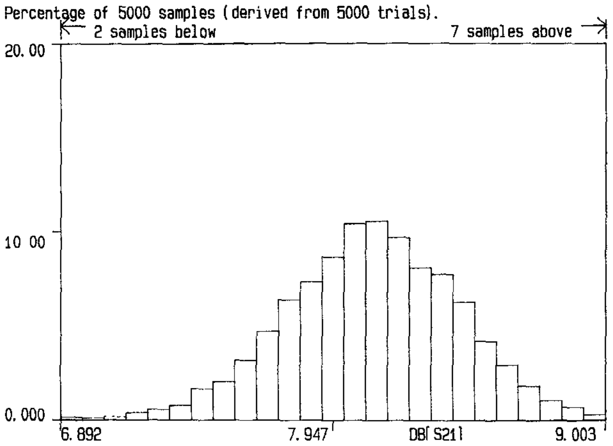

Figure 5. Performance Histogram for Gain

deviation is 0.22 dB less than the measured and is most likely due to under estimating the standard deviation for DPHIS. Overall, there is an excellent agreement in the predicted versus measured mean and standard deviation in gain versus frequency. Good agreement was also achieved between the predicted versus measured performance for other parameters such as the input return loss as shown in Figures 6 and 7. Using a yield requirement of 6.5 dB < G < 9.0 dB for a 2- to 18-GHz bandwidth, the RF yield of this low-noise amplifier was predicted at 93 percent.

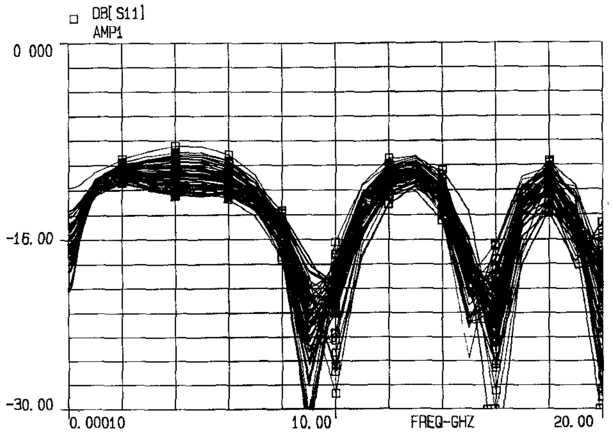

Figure 6. Predicted Return Loss Variation

CONCLUSION

In summary a new technique for computing predicted small-signal RF yield of a MMIC circuit design based on physical parameters has been described. This technique uses commonly measured FET physical parameters in conjunction with electrical parameter sensitivity equations to model both passive and active circuit elements. A linear microwave circuit simulator is then used to compute the RF yield through Monte Carlo analysis. This RF yield analysis method has successfully been applied to several MMIC amplifiers with good results between measured and computed performance. Future work is in progress to adapt this technique to large-signal microwave circuits.

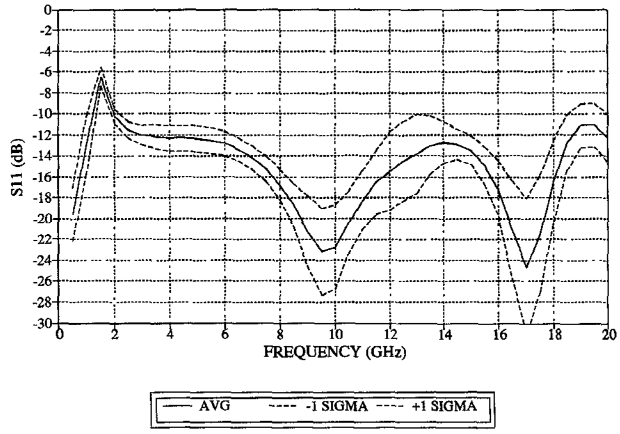

Figure 7. Measured Input Return Loss Variation

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